Pixel CMOS Design Using Current-Mirror Circuit

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Abstract

This paper explains a study on several photodiodes sensors including current mirror amplifiers. These photodiodes have been fabricated using a CMOS 0.6 micrometers process from Austria Mikro Systeme (AMS). Each sensor pixel in the array occupies respectively, 1mm x 1mm area, 0.5mm x 0.5mm area and 0.2mm 0.2 mm area with fill factor 98 % and total chip area is 2 square millimeters. The sensor pixels show a logarithmic response in illumination and are capable of detecting very low green light emitting diode (less than 0.5 lux). These results allow using our sensor in new Gamma Camera solid-state concept.

Keywords: CMOS, current-mirror, sensor, pixel

INTRODUCTION

CMOS (Complementary Metal Oxidizes Semiconductor) Sensors intended for imagery cause much interest for industrial applications and research. Sensors based on this technology exceed the traditional sensors based on CCD (Charge Coupled Device) technology. CMOS sensors offer many advantages. It offers weak manufacturing cost compared to a CCD sensor, integration facility of multiple functionalities intended for imagery, high space resolution, and pixels random access. Some disadvantages of CMOS sensors compared to CCD sensor are noise of reading which is more important and sensitivity which is less important. CMOS imaging sensors use active or passive pixels, as depicted in Figure 1 and Figure 2. Active-pixel sensors (APS) include amplification circuitry in each pixel.

Active-pixel sensors make use of active transistor to buffer signal output within the pixels and drive the readout circuitry of the pixel arrays. The array themselves can be made very flexible. Currently under consideration

Figure 1. CMOS Sensors with Passive Pixels

Figure 2. CMOS Sensors with Active pixels
is an array of active-pixel sensors that can be readout one row at a time. A column of row registers addresses each of the pixels in a row, each of which then sends output to a bottom row of column registers and adjacent analog circuitry. The pixel circuitry can use this photo-current. The photocurrent of an ordinary photodiode is very small; a charge integration based operation is common in many active pixel sensors. In this context we designed a new CMOS image sensor array that presented in this article. Operation of current mirror is introduced in the second section. The third and fourth sections describe the design of CMOS Active Pixel Sensor using current-mirror circuit. In the fifth section, the paper concludes with fabrication and test results about this new sensor.

RESEARCH METHODS

The first research phase of this design is the design of current-mirror to sensor photodiode. The second phase is simulation of the current-mirror using mentor graphic. Furthermore, design of the layer structure photodiode evaluates several sizes: 1 mm x 1 mm, 500 mm x 500 mm, 200 mm x 200 mm. The objective is to identify the best light sensitivity of these sensors measure. The next phase is to unite the current-mirror circuit with photodiode to form a pixel. Pixels that have been put together and designed for the fabrication, all this is done using mentor graphics software. The final step is testing and analysis of pixel fabrication results.

DISCUSSION

The Operation of Current Mirror

The basic idea of the design is illustrated in Figure 3. The capacitance C consists of the capacitance of any connected device at the node V plus the photodiode junction capacitance itself. When light illuminates the photodiode, the reverse photocurrent discharges the output node V, therefore we can write Equation 1. For a n+ - p diode with ND >> NA, the junction capacitance is given by Equation 2. In Equation 2, A is the diode area, NA is the acceptor concentration in the substrate, and ND is the doping concentration of the n+ region. Combining Equations 1, 2, and integrating we find Equation 3, where \( V_{\text{reset}} \) is the reset reserve bias. Solving for \( V(t) \), we get Equation 4.

\[
C(V) \frac{dV(t)}{dt} = -i_{\text{photo}}. \tag{1}
\]

\[
C(V) = \frac{A}{2} \left[ \frac{2q\varepsilon_S N_A}{V(t)} \right]^{1/2}. \tag{2}
\]

\[
A \left[ \frac{2q\varepsilon_S N_A}{V(t)} \right]^{1/2} \left[ \frac{2V}{V(t)} \right]^{V(t)+V_h} = -i_{\text{photo}}. \tag{3}
\]

\[
V(t) = \left[ V_{\text{reset}} - \frac{i_{\text{photo}}}{A(2q\varepsilon_S N_A)^{1/2}} \right]. \tag{4}
\]

When \( V(t) \) is plotted as a function of time, linearity in the output is observed for a time period. Worthy noting is that since \( i_{\text{photo}} \propto I_{\text{ph}} \), the dependence on photodiode area cancels out. In general, a large photodiode area with high fill factor is desired. These are several advantages in using integration-mode: charge integration, low parasitic on sense node, voltage multiplexing, no kT/c noise and low dark current. On the other hand, the disadvantages are smaller fill factor and more complicated addressing.
Current Mirror Principles in nMOS

Figure 3

Current Mirror Principles in pMOS

Figure 4

Current-Readout Pixels Operation

Current readout active pixel sensors are inherently advantageous in terms of readout speed because the fixed output line voltage at input of trans-resistance amplifier prevents charge-discharge phenomena. Another benefit of current readout is current-mode processing which is relatively compact in size and simple in its operations. In current-mode, the photo-current of detector can be mirrored and readout directly.

The Current Mirror

The current mirror is one of the most useful basis block in analog design. In its most simple configuration, it consists in two MOS devices as in Figure 3 and Figure 4.

A current $I_{ref}$ flowing through the nMOS device M1 is copied to the nMOS device M2. If the size of M1 and M2 are identical, in most operating conditions, the current are the same. The remarkable point is that the current is almost independent of the drain voltage of the M2 V2. If the ration W/L of the M2 is 10 times the ratio of the M1, the current on the right branch is 10 times the current on the left branch. The formula when M1 operates in saturation is shown in Eq 5 below. Equation 6 and 7 shows if M2 operates in saturation.

$$I_{ref} = I = \frac{k}{2} \left( \frac{W}{L} \right) (V_{GS1} - V_{TH}) (1 + \lambda V_{DS1})$$  \(5\)

$$I_{out} = I_2 = \frac{k}{2} \left( \frac{W}{L} \right) (V_{GS2} - V_{TH}) (1 + \lambda V_{DS2})$$  \(6\)

$$I_{out} = I_{ref} \left( \frac{W}{L} \right) (1 + \lambda V_{DS2})$$  \(7\)

The Design of Current-mirror CMOS Pixels

Figure 5 shows a block diagram and Figure 6 shows layout of small test chip implemented in a standard 0.6 μm CMOS process. This is the first step to realize a gamma-camera on-a-chip. The chip consists mainly of current-mirror active pixels size: (a) 1x1 mm2 (the two pixels), (b) 500x500 μm2 (the four pixels) and (c) 200x200 μm2 (the eight pixels), each constituted of a
photodiode with control switch and current output amplifying circuitry.

**Pixel Circuit**

The pixel circuit is shown in Figure 7. Here, the current mirror (M1 and M2) is designed such that W2 = 2 x W1. The photocurrent is thus amplified 10 times.

The output current gain of this simple current mirror is finite, as a result. For increasing of current gain, in this design we added on nMOS-pMOS combination of current-mirror circuits. M9 is used as switch, when COM (M9) is on, pixel current is output to the column, as in Figure 8.

We create of photodiode type N as in figure 9. The cathode of photodiode N, the cathode of the photodiode consist of a square of diffusion connected on all its circumference by a whole of contacts connected in crown. This provision makes it possible to reduce the resistance of the contacts. The anode was carried out by surrounding the photodiode of a ring of polarization of the substrate, this to limit the resistive effects of the substrate. The contacts of these two crowns are carried out with the minimum step authorized by technology.

**Simulation and Layout Current-Mirror CMOS Circuit**

For the simulation of our circuit current-mirror CMOS, we called upon a software of computer-aided design called

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**Figure 5. Block Diagram of Current-mirror CMOS Pixels**

**Figure 6. Layout of Current-mirror CMOS Pi:**
Mentor Graphics. By the intermediation of the software Design Architect version AMS (Austria Mikro System), we can carry out the seizure of our diagrams electronics directly in technology CMOS. Accusim enables us to simulate our diagrams carried out. After that we use the software IC-Station version LY or PR for the design of the layout of electronic diagrams. Given the complexity of the software IC-Station, we have created a manual, allowing the user to familiarize itself with the manual routing suggested by AMS. The technology used is a technology CMOS of 0.6 micron. To be able to process the data provided by the photodiode, we tested circuits allowing the amplification and the selection of our signal.

In Figure 10, we added two more CMOS (nMOS (M10) and pMOS (M11)). Its aim is to see the output of this circuits, before or after the amplifying. The circuit has two switch (sw and com) and two output (direct and sortie). Figure 11 is diagram of layout the current-mirror with combination nMOS and pMOS.

The circuit operation is very simple. First, the current Iphoto passes through M1 and is mirror to M2 using current mirror. If the HIGH signal is given to switch SW and COM, the results obtained at the output DIRECT, that is before the current Iphoto is amplified by the current-mirror with combination nMOS and pMOS. If the LOW signal is given to switch SW and COM, the results at output SORTIE, that is after the current Iphoto is amplified by the current-mirror with combination nMOS and pMOS.

For simulation purpose, we used a calibrated current of 0A with 200nA. From the results of simulation, it is visible that the current-mirror circuit with combination nMOS and pMOS to achieve a high current gain.

**Fabrication and Test Results**

Figure 12 shows a block diagram and Figure 13 shows photograph of small test pixels implemented in a standard 0.6 μm CMOS process from AMS. The chip consists...
Figure 11. Diagram of Layout The Current-Mirror with Combination Nmos and Pmos

Figure 13. Photograph of photodiode Sensors

Table 1. The measurement characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.6 μm CMOS, 2-layer Metal et 1-layer Poly</td>
</tr>
<tr>
<td>Photodetector</td>
<td>Diffusion N+/P Substrat</td>
</tr>
<tr>
<td>Sensor Area</td>
<td>2 mm x 2 mm</td>
</tr>
<tr>
<td>Pixel Pitch</td>
<td>1 mm x 1 mm, 0.5 mm x 0.5 mm, and 0.2 mm x 0.2 mm</td>
</tr>
<tr>
<td>Fill Factor</td>
<td>98%</td>
</tr>
<tr>
<td>Spectral Response</td>
<td>700 nm (RED) and 585 nm (GREEN)</td>
</tr>
<tr>
<td>Power Supply</td>
<td>5 Volt</td>
</tr>
<tr>
<td>Response in Illumination</td>
<td>Logarithmic</td>
</tr>
</tbody>
</table>
mainly of current-mirror active pixels with different sizes: (a) 1x1 mm² (the two pixels: u and v), (b) 500x500 μm² (the four pixels: q, r, s and t) and (c) 200x200 μm² (the sixteen pixels: a - p), each constituted of a photodiode with control switch and current output amplifier circuits.

The photo response of test photodiodes on the chip is obtained by measuring the photo current under illumination (Lux) from green and red light emitting diode. Table 1 summarizes the overall measurement characteristics.

Table 1

<table>
<thead>
<tr>
<th>Lux of Green LED</th>
<th>Output Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1</td>
<td>0.2</td>
</tr>
<tr>
<td>0.2</td>
<td>0.4</td>
</tr>
<tr>
<td>0.3</td>
<td>0.6</td>
</tr>
<tr>
<td>0.4</td>
<td>0.8</td>
</tr>
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</table>

Figure 14 and 15 shows variations output voltage with light intensity of green and red lights emitting diode. It shows a logarithmic relation of output signal in function of emitting light (Lux).

The test result also shows variations of photo current in dynamic mode. In this mode, light emitting diode is driven with a pulse generator. Results presented in Figure 16 and 17 are obtained with a green LED calibrated for a 0.4 lux illumination. Results shown in Figure 18 and 19 are obtained with a red LED calibrated for a 0.3 lux illumination. In these
Conclusions and Perspectives

A 2 square millimeters area of CMOS active photodiode sensor with current mirror amplifier has been fabricated using a 0.6 μm CMOS process. The experimental results show that this sensor has logarithmic response in illumination and is capable of detecting very low green lights emitting diode. These results allow us to consider using of this technology in new solid state gamma cameras.

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